What is Claimed is:

1. A method of operating a digital system having a processor and associated translation lookaside buffer (TLB), comprising the steps of:

executing a plurality of program tasks within the processor;

initiating a plurality of memory access requests in response to the plurality of program tasks;

caching a plurality of translated memory addresses in the TLB responsive to the plurality of memory access requests;

incorporating a task identification value with each translated memory address to identify which of the plurality of program tasks requested the respective translated memory address;

incorporating a shared indicator with each translated memory address to indicate when a translated memory address is shared by more than one of the plurality of program tasks; and

invalidating a portion of the plurality of translated memory address in the TLB in a manner that is qualified by the shared indicator.

2. The method according to Claim 1, wherein the step of invalidating comprises invalidating a translated memory address only if it is shared.

3. The method according to Claim 1, wherein the step of invalidating comprises invalidating a translated memory address only if it is not shared.

4. The method according to Claim 1, wherein the TLB has several levels, and wherein the step of invalidating encompasses all of the several levels of the TLB.

5. The method according to Claim 1, wherein the step of invalidating is qualified by both the shared indicator and the task identification value.

6. The method according to Claim 1, further comprising the step of incorporating a second qualifier value with each translated memory address; and

wherein the step of invalidating is qualified by both the shared indicator and the second qualifier value.

7. The method of Claim 6, wherein the digital system has a plurality of processors and wherein the second qualifier value identifies which of the plurality of processor requested the respective translated memory address.

8. The method according to Claim 4, wherein the step of invalidating comprises invalidating all shared entry locations of the plurality of translated memory address in the TLB in response to a single command issued from the processor.

9. The method according Claim 1, further comprising the steps of:

maintaining a set of page translation tables for providing each translated memory address; and

including within the set of page translation tables the shared indicator for each translated memory address.

10. The method according to Claim 1, further comprising the step of maintaining a set of page translation tables for providing each translated memory address, wherein the shared indicator for each translated memory address is not included within the set of page translation tables.

11. The method according to Claim 1, wherein a shared translated memory address is replicated in the TLB for each program task that requests it.

12. The method according to Claim 1, wherein the plurality of program tasks exist in a same address space, and wherein the step of caching comprises caching in the TLB only a single copy of a shared translated memory address.

13. The method according to Claim 12, wherein the task identification value of a shared translated memory address is ignored.

14. A digital system having a translation lookaside buffer (TLB), the TLB comprising:

storage circuitry with a plurality of entry locations for holding translated values, wherein each of the plurality of entry locations includes a first field for a translated value and a second field for an associated shared indicator;

a set of inputs for receiving a translation request;

a set of outputs for providing a translated value selected from the plurality of entry locations; and

control circuitry connected to the storage circuitry, wherein the control circuitry is responsive to an operation command to invalidate selected ones of the plurality of entry locations according to the shared indicator.

15 The digital system of Claim 14, wherein the digital system further comprises a second level TLB connected to the TLB, the second level TLB comprising:

second level storage circuitry with a plurality of entry locations for holding translated values, wherein each of the plurality of entry locations includes a first field for a translated value and a second field for an associated shared indicator; and

wherein the control circuitry is connected to the second level storage circuitry, the control circuitry being responsive to an operation command to invalidate selected ones of the plurality of entry locations in the second storage circuitry according to the shared indicator, such that qualified entry locations in the TLB and in the second level TLB are invalidated in response to a single operation command.

16. The digital system according to any of Claim 14 being a personal digital assistant, further comprising:

a processor (CPU) connected to the TLB and thereby connected to access a memory circuit;

a display, connected to the CPU via a display adapter;

radio frequency (RF) circuitry connected to the CPU; and

an aerial connected to the RF circuitry.